## REMARKS

This Response is responsive to the non-final Office Action mailed October 30, 2008. Claims 1-6, 8, 25-28, and 34 are pending. Claims 1, 25, 28, and 34 have been amended. In view of the following remarks, as well as the preceding amendments, Applicants respectfully submit that all claims in this application are in complete condition for allowance and request reconsideration of the application in this regard.

**Rejections of Claims Under 35 U.S.C. § 112**

Claims 1-6, 8, 25-28 and 34 stand rejected under 35 U.S.C. § 112, 2nd paragraph. Applicants have amended these claims in a manner believed sufficient to overcome the rejection.

**Rejections of Claims Under 35 U.S.C. § 103**

Claims 1-6, 8, 25-28, and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,566,704 to Choi et al. (hereinafter *Choi*). Claims 1 and 25 are independent claims. Applicants respectfully disagree with this rejection for the reasons set forth below.

In determining the differences between the prior art and the claims, the question under 35 U.S.C. § 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. In this instance, Applicants submit that the claimed inventions set forth in claims 1 and 25 would not have been considered obvious when considered as a whole.

With regard to independent claim 1, the Examiner states that "*Choi* et al. do not explicitly state in the embodiment of figure 3F a plurality of semiconducting nanotubes." However, to support the rejection, the Examiner contends that:

> Choi et al. teach using a plurality of semiconducting nanotubes in the disclosed invention of nano sized transistor (see, for example, column 3, lines 39-43), wherein figures 1-3 depict only a unit cell of the transistor (column 3, lines 41-43). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a plurality of semiconducting nanotubes having a plurality of dielectric layers in Choi et al.'s device in order to use the device in a practical application which requires a plurality of semiconducting nanotubes having a plurality of dielectric layers, such as a nano sized transistor.

Initially, this contention by the Examiner fails to amount to objective reasoning sufficient to support the modification. The Examiner is arguing that it would have been obvious "to use a plurality of semiconductor nanotubes ... in a practical application which requires a plurality of semiconducting nanotubes." This circular logic fails to amount to objective reasoning in the manner required by MPEP § 2143.

Applicants further submit that the general statements regarding the plural term "carbon nanotubes" made at column 3, lines 39-41 of *Choi*, or for that matter any other similar general statement made in *Choi*, fails to support a conclusion that the unit cell described in the context of Figures 1-3 of *Choi* can be modified to include more than one semiconducting nanotube.

*Choi* describes the unit cell shown in each of Figures 1-3 as including a nano-sized hole (10') and a nanotube (100) with a nano-sized diameter. *See* col. 3, lines 44-60. Hence, the nanometer dimensions of the hole (10') and the nanotube (100) are arguably commensurate. *Choi* fails to explicitly disclose or suggest that the dimensions of the hole (10') can be increased to accommodate multiple semiconducting nanotubes (100), much less that the hole (10') can accommodate more than one nanotube (100) without any modification in the dimensions. Hence, without further elaboration by the Examiner, Applicants submit that the general statements found at column 3, lines 39-41 of *Choi* fail to objectively lead to the conclusion drawn by the Examiner that the unit cell shown in Figures 1-3 of *Choi* can be modified to include multiple semiconducting nanotubes.

Moreover, the Examiner's conclusion that each unit cell shown in Figures 1-3 of *Choi* can include multiple semiconducting nanotubes is based solely upon the hindsight provided by Applicants' own specification. Impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art, which in this instance is the specification of *Choi*. For reasons explained below, the Examiner's reasoning takes into account knowledge which was not within the level of ordinary skill in the art at the time the claimed invention was made and includes knowledge gleaned only from Applicants' specification.

The Examiner's position that "to use the device in a practical application ... requires a plurality of semiconducting nanotubes" is believed by the Applicants to apply to the use of the unit cell shown in Figures 1-3 of *Choi* in a setting that includes multiple unit cells. Even if a

person having ordinary skill in the art were to replicate the single nanotube unit cell shown in Figures 1-3 of *Choi* to make multiple unit cells, each of the individual unit cells would still only include a single semiconducting nanotube (100) with a channel current flow regulated by a control voltage from a gate electrode (20). Applicants' claim 1 sets forth that the device structure includes a plurality of semiconducting nanotubes and that each of the semiconducting nanotubes has a current flow through its channel region regulated by a control voltage from the claimed gate electrode.

According to MPEP § 2143, the prior art can be modified or combined to reject claims as *prima facie* obvious as long as there is a reasonable expectation of success. In this instance, a person having ordinary skill in the art would not have appreciated from the disclosure associated with column 3, lines 39-43 of *Choi*, or the disclosure in any other passage of *Choi*, that a reasonable expectation of success exists to modify the structure shown in Figure 3F of *Choi*, as proposed by the Examiner. The passage at column 3, lines 39-43 of *Choi* reads:

> A vertical nano-sized transistor using carbon nanotubes according to the first embodiment of the present invention will now be explained. As shown in FIG. 1, a unit cell of a vertically aligned carbon nanotube transistor is constructed as follows.

The two sentences within this passage are contradictory and internally inconsistent in that the first sentence refers to nanotubes plural, but the second sentence refers to nanotube in the singular. The former sentence fails to state that each transistor includes more than one carbon nanotube. The latter sentence is consistent with the description in *Choi* that follows in connection with Figures 1-3.

The intrinsic evidence in *Choi* fails to teach a person having ordinary skill in the art how to modify the device shown in Figures 1-3 to include a plurality of nanotubes. This is not an obvious modification that a person having ordinary skill in the art would have made to the device structure of Figure 3F based upon the Examiner's allegedly objective reasoning and with a reasonable expectation of success

For at least these reasons, Applicants submit that the Examiner has failed to properly support a case of *prima facie* obviousness with regard to independent claim 1. Therefore, Applicants respectfully request that the Examiner withdraw this rejection.

Because claims 2-6 and 8 depend from independent claim 1, Applicants submit that these claims are also patentable for at least the same reasons discussed above. Furthermore, these dependent claims recite unique combinations of elements not disclosed or suggested by *Choi*.

Independent claim 25 recites that each of the dielectric layers has "a second portion disposed between one of said nanotubes and said second plate". In contrast, *Choi* discloses that the "[t]he lower and upper parts of each carbon nanotube are connected to a source and a drain, respectively, with a gate interposed between the source and the drain for performing switching". *See* col. 1, lines 55-58. The Examiner identifies the claimed dielectric layer as the object labeled with reference numeral (30) in *Choi* and the claimed second plate as the object labeled with reference numeral (50) in *Choi*. One end of the nanotube (100) is connected with the second plate (50). No portion of the dielectric layer (30) is disposed between this end of the nanotube (100) and the second plate (50).

Consequently, under the framework of the *Graham* factual inquiries, *prima facie* obviousness has not been established because there are unresolved differences between independent claim 25 and the disclosure in *Choi*. Specifically, *Choi* fails to disclose that each of the dielectric layers has "a second portion o disposed between one of said nanotubes and said second plate". For at least this additional reason, Applicants respectfully request that the Examiner withdraw the rejection.

Independent claim 25 is patentable for at least an additional reason. Specifically, similar to independent claim 1, Applicants' independent claim 25 recites a plurality of nanotubes. Applicants hereby incorporate by reference the arguments presented above with regard to the rejection of claim 1 as to the objective reasons that a person having ordinary skill in the art would not have modified the device structure shown in Figure 3F of *Choi* to include multiple nanotubes. Under the framework of the *Graham* factual inquiries, the Examiner has failed to establish *prima facie* obviousness because there are unresolved differences between independent claim 25 and the disclosure in *Choi*. For at least this additional reason, Applicants request that the rejection be withdrawn.

Because claims 26-28 depend from independent claim 25, Applicants submit that these claims are also patentable for at least the same reasons discussed above. Furthermore, these dependent claims recite unique combinations of elements not disclosed or suggested by *Choi*.

**Rebuttal to Examiner's "Response to Arguments"**

On page 9 of the Office Action, the Examiner contends that "Applicant argues that there is no motivation to form plurality of nanotubes in Choi's device". Applicants are arguing that the intrinsic evidence in *Choi* fails to provide an objective reason that would have caused a person having ordinary skill in the art to modify the device shown in Choi to include a plurality of nanotubes.

The Examiner states that the "combination is not based upon hindsight, because Choi et al. teach a transistor using carbon nanotubes." In Figure 3F, *Choi* teaches a transistor that includes a single carbon nanotube. *Choi* fails to teach that the transistor in Figure 3F can include more than one carbon nanotube. The only teaching of a device structure, as set forth in claims 1 and 25, that contains multiple carbon nanotubes is found in Applicants' specification.

The Examiner states that "[s]ince Choi et al. teach a transistor using carbon nanotubes, it is understood that Choi et al. teach plurality of unit cells". The Examiner then states "[a]lthough each of the individual unit cells would still include only a single semiconductor nanotube". Hence, the Examiner apparently recognizes that each transistor in *Choi* includes a single nanotube.

In Applicants' claim 1, a plurality of nanotubes is associated with each semiconductor device structure and each of the nanotubes has a single channel region. Claim 1 recites that "each of said semiconducting nanotubes" includes "a channel region extending vertically through said gate electrode between said source region and said drain region" and the gate electrode regulates "current flow through said channel region between said source region and said drain region". Hence, the semiconductor device structure in claim 1 has multiple channel regions. In comparison, each semiconductor device structure in *Choi* includes one nanotube and one channel region.

The Examiner states that he "does not suggest to modify the device structure of Figure 3F"and that "the examiner does not suggest increasing the dimensions of the hole (10') to accommodate multiple semiconducting nanotubes (100)". To the contrary, the Examiner contends that the entire subject matter of independent claim 1, but for the plurality of semiconducting nanotubes, is found in the device structure shown in Figure 3F of *Choi*. The Examiner is attempting to modify the device structure of Figure 3F in *Choi* from a single

semiconducting nanotube construction to a construction that includes multiple semiconducting nanotubes. Choi's device construction in Figure 3F is tailored to have a single nanotube. Applicants are attempting to rebut the Examiner's attempted modification to *Choi* by demonstrating with objective reasoning that a person having ordinary skill in the art would not have made this modification to the structure of Figure 3F in *Choi*.

**Conclusion**

Applicants have made a bona fide effort to respond to each and every requirement set forth in the Office Action. In view of the foregoing remarks, this application is submitted to be in complete condition for allowance and, accordingly, a timely notice of allowance to this effect is earnestly solicited. In the event that any issues remain outstanding, the Examiner is invited to contact the undersigned to expedite issuance of this application.

Applicants do not believe fees are due in connection with filing this communication. If, however, any fees are necessary as a result of this communication, the Commissioner is hereby authorized to charge any under-payment or fees associated with this communication or credit any over-payment to Deposit Account No. 23-3000.

Respectfully submitted,

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